

REMARKS

Pending Claims:

In this application, claims 1, 4, 5, 7-12, 14, 18, 23-35 are currently pending. Claims 1, 4, 5, 7-11, 14, 18, and 23-24 are amended by this Response. Claims 12, 13, 16, and 17 remain unchanged since filing. Claims 2, 3, 6, 15, and 19-22 have been deleted. Claims 25-35 have been added. Entry of these amendments is respectfully requested.

Rejection under 35 U.S.C. §102 and 35 U.S.C. §103

The Examiner has rejected claim 18 as being anticipated by Yamada (U.S. Patent No. 5,455,820). The Examiner rejected all other claims (1-17, 19-24) as being obvious under section 103 in light of Yamada and Yamanka (U.S. Patent No. 5,619,495), with some of these claims being rejected as obvious also in light of Merchant (U.S. Patent No. 6,904,043) and/or Caldara (U.S. Patent No. 5,978,359).

Cited Prior Art References

The primary reference for teaching the existence of deferred buffers for the avoidance of head of line blocking is the Yamada reference. Yamada teaches an ATM switch with input and output buffers where a signal sent to all input ports indicates that the output buffers are full or nearly. When a new cell is received at the input that is destined for an output port that has a full buffer, the cell is placed in a separate spare buffer. That spare buffer is allocated only for that single output port. If another output port buffer becomes full, cells destined for that port would be placed in a different spare buffer. When a formerly unavailable port becomes available, a buffer selector begins selecting cells from the spare buffer as well as the main buffer. When the spare buffer becomes empty, it becomes available for the next port having a full output buffer.

The Yamanka reference is cited for teaching a switch with dual port buffers and associated buffer write and read modules. No teaching is provided in Yamanka for the use of deferred queues that can avoid head of line blocking. Similarly, Caldara is cited for the use of an "XOFF mask" to determine the current status of destination ports in a buffered switch. The applicant acknowledges that Caldara teaches a data switch in which internal flow control is accomplished by submitting XOFF and XON signals from egress ports to ingress ports. However, the applicant notes that Caldara does not teach a bit mask where each bit represents the state of a separate output port. In addition, like

Yamanka, Caldara does not teach any technique for avoiding head-of-line blocking at the ingress port.

Merchant stores all incoming data frames in a single, external memory. Copies of the frame headers are stored for each incoming frame in an input queue structure along with pointers to the frame location in the external memory. The routing engine determines the egress port for each frame, and then places the frame header and memory address pointer in an egress queue for that port. From there, the frame header is read off of the output queue, and the data frame is located in the external memory and then output out of the egress port. The only flow control discussed in Merchant occurs when an input queue for a receive port becomes full. In this case, the switch implements flow control through the receive port, the process for which is not described within the Merchant reference. Consequently, while Merchant does teach the use of queues containing header information and a memory pointer to track data within a switch, Merchant does not teach the use of the “deferred” queue that can avoid head-of-line blocking as claimed in the present invention.

Claim Elements in the Newly Amended Claims that Distinguish Over the Prior Art

The only deferred queue structure found in the cited prior art is Yamada, which teaches a separate queue or cell buffer for each blocked destination port. This is similar to the dedicated queue structure described in the background of the prior art section of the present application at paragraph [0004]. The main difference is that the structure described at paragraph [0004] dedicates a separate queue for every destination port, while Yamada has a more flexible structure that allocates a separate queue only when a particular port is determined to be blocked. While this is an improvement over the prior art described at paragraph [0004], Yamada still requires that every blocked port be allocated a separate queue (or cell buffer 140) at the input port. This requires the creation and maintenance of enough cell buffers 140 to account for the maximum number of blocked egress ports. Failure to provide enough cell buffers would result in the loss of data cells. Yamada, col. 4, lines 61-66.

The present invention avoids this overhead and possible data loss by placing all deferred data in a single deferred queue. Data that is addressed to multiple, blocked destination ports is stored in a single data structure. This ability limits the number of separate queues required to avoid head-of-line blocking, which in turn reduces queue

overhead and physical memory requirements. Nothing in Yamada or any of the other cited references teaches this unique ability.

Newly amended claim 1 now requires a deferred queue “with entries for data addressed to multiple destinations ports being intermingled within the deferred header queue.” Similarly, independent claim 10 states that “the deferred header queue device [contains] packets/ frames addressed to more than one destination port” and independent method claim 18 requires “storing the data in a deferred queue whereby data addressed to different destination ports are simultaneously stored in the same deferred queue.” In this way, all of the original claims have been amended to include this element, and are patentable over the prior art.

One requirement of having a single structure contain deferred data for multiple destination ports is a capacity to transmit over the switch that data in the structure that is addressed to a now available destination port while keeping within the structure other data that is addressed to still-blocked ports. This requirement, which is found nowhere in the prior art, is also found in the amended independent claims 1 and 18. Consequently, this element provides a separate rationale for allowance of these claims.

The present invention also includes a backup queue to handle data that is received at an input port when a deferred queue is being processed. While Yamada teaches multiple deferred queues or buffers, the cell buffers 140 are not utilized to handle incoming data when the deferred queue is being processed, and therefore have a separate functionality and use compared to the present invention. Amended claims 5, 11, 12, 23, and 24 now explicitly distinguish the backup queue of the present invention from the spare cell buffers of Yamada.

Finally, the present invention handles the processing of the queues and incoming data differently depending upon the state of an internal state machine. The use of a state machine in this context is not described in any of the prior art references, and is explicitly claimed in independent claims 1 and 18, and dependent claims 11 and 23.

New Claims:

Claims 25-35 are new claims that are supported by the specification as originally filed. Claim 25 is a dependent claim depending from claim 18 defining the content of the deferred queue. Claim 26 is a new independent claim explicitly claiming a state

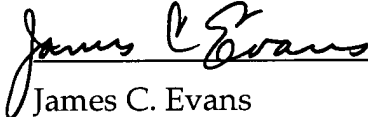
machine. Claims 27-34 are dependent claims stemming directly or indirectly from new claim 26. Claim 35 is a new independent claim reciting a deferred queuing means and a logic unit having an initial and a deferred state. These claims are also patentable over the prior art.

CONCLUSION

All of the claims remaining in this application should now be seen to be in condition for allowance. The prompt issuance of a notice to that effect is solicited.

Respectfully submitted,
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